In the Specification

Please amend the Title beginning on page 1, line 1 as follows:

~~PROCESSOR INTERFACE~~PROCESSING SYSTEM STREAMING DATA HANDLING SYSTEM AND STREAM REGISTER

Please amend the paragraph beginning on page 5, line 28 as follows:

Whilst the system of figures 1, 2 and 2a is advantageous in that it is simple, avoids the need for complicated software and provides an improvement in the speed of returning data to the CPU 2 over some known systems, it can suffer from a couple of disadvantages. Firstly, if a data item requested by the execution unit 27 of the CPU 2 does not become available during a large number of clock cycles, say about ~~10 000~~ten thousand, there is a risk that such an excessive delay will eventually result in irrecoverable stalling of the execution unit of the CPU 2, due to there being no control mechanism to deal with this situation. This would result in the user of the system needing to switch the CPU 2 off and on again to allow the CPU 2 to reset. Another consideration is that there is no mechanism for signalling an interrupt to the execution unit 27 of the CPU 2 while it is stalled. If an interrupt were able to be signalled by a timeout mechanism, it would allow the execution unit 27 of the CPU 2 to perform other tasks while it waited for the missing data item, which would increase overall efficiency of the system 1. To deal with these issues, a second embodiment, is shown in figure 3.